

FIG. 1A

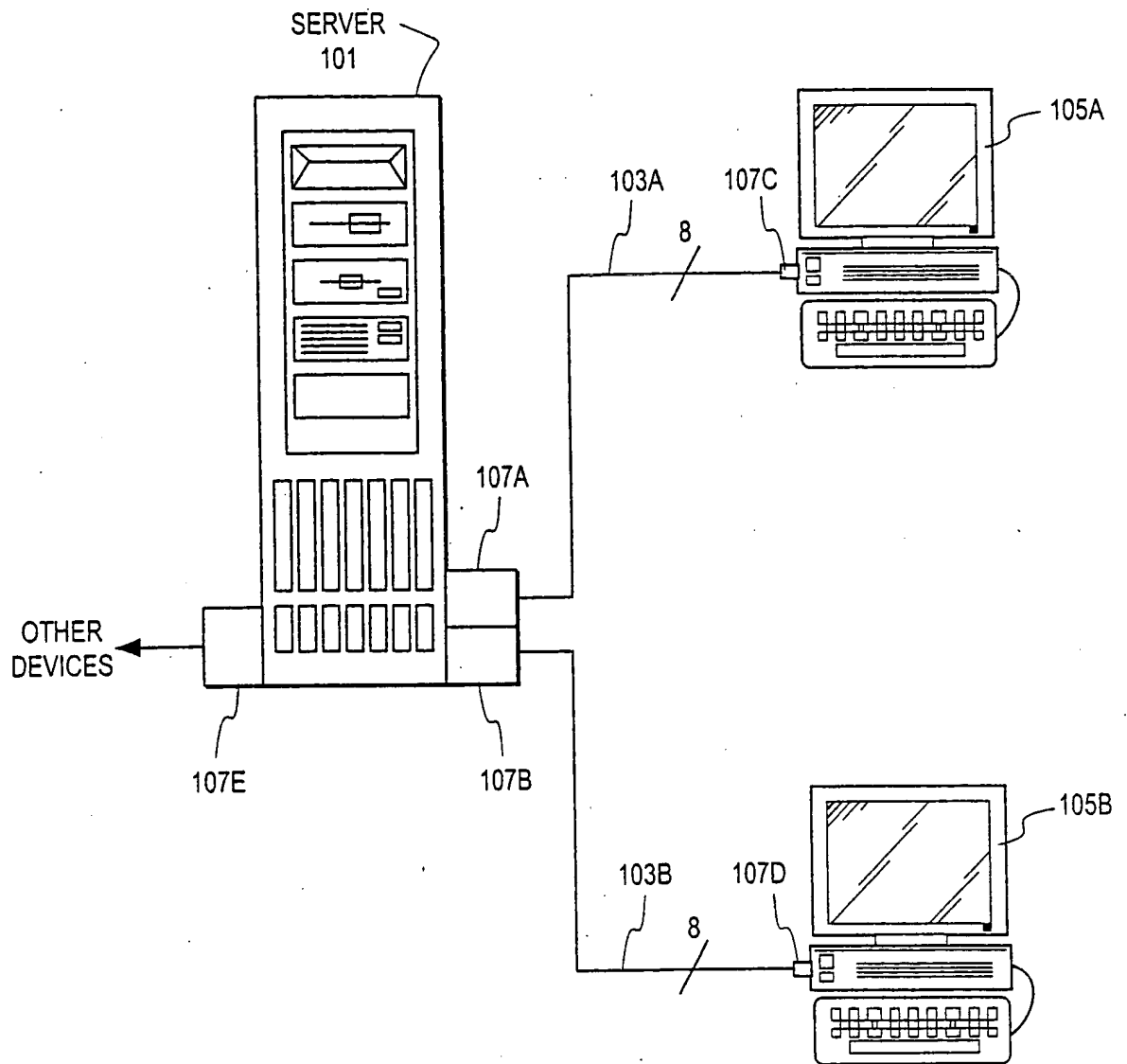
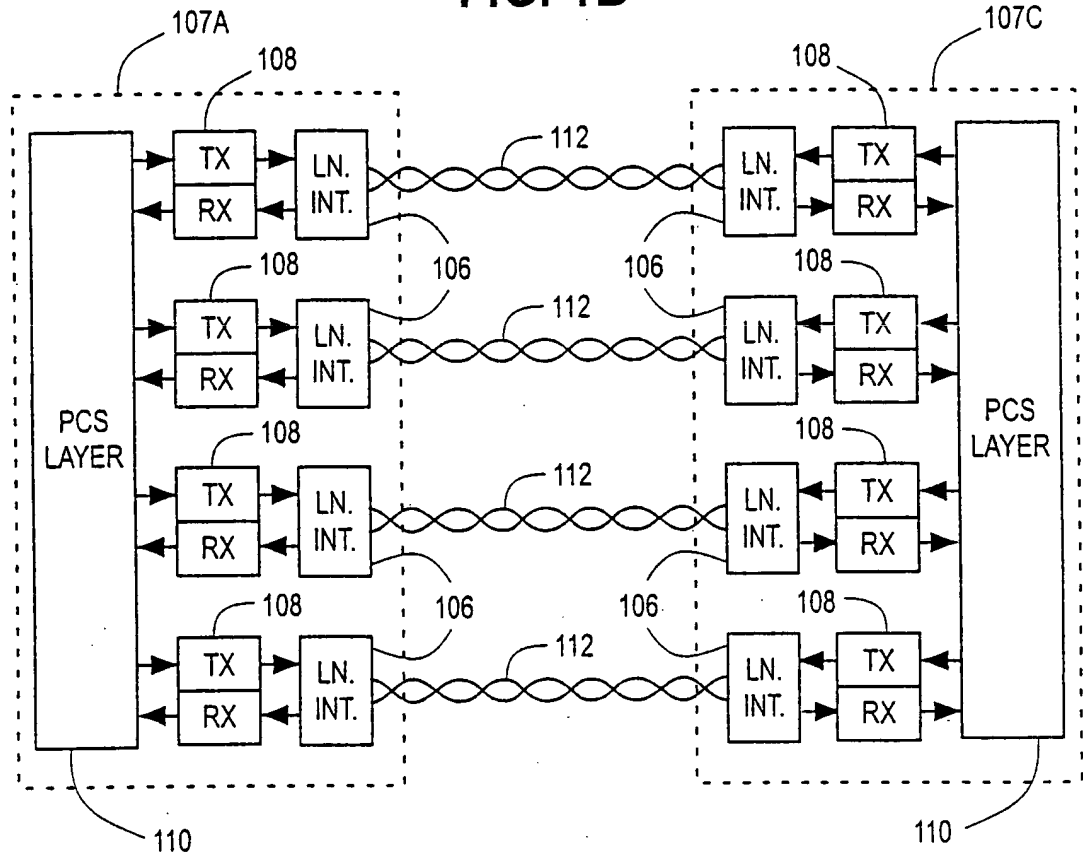


FIG. 1B



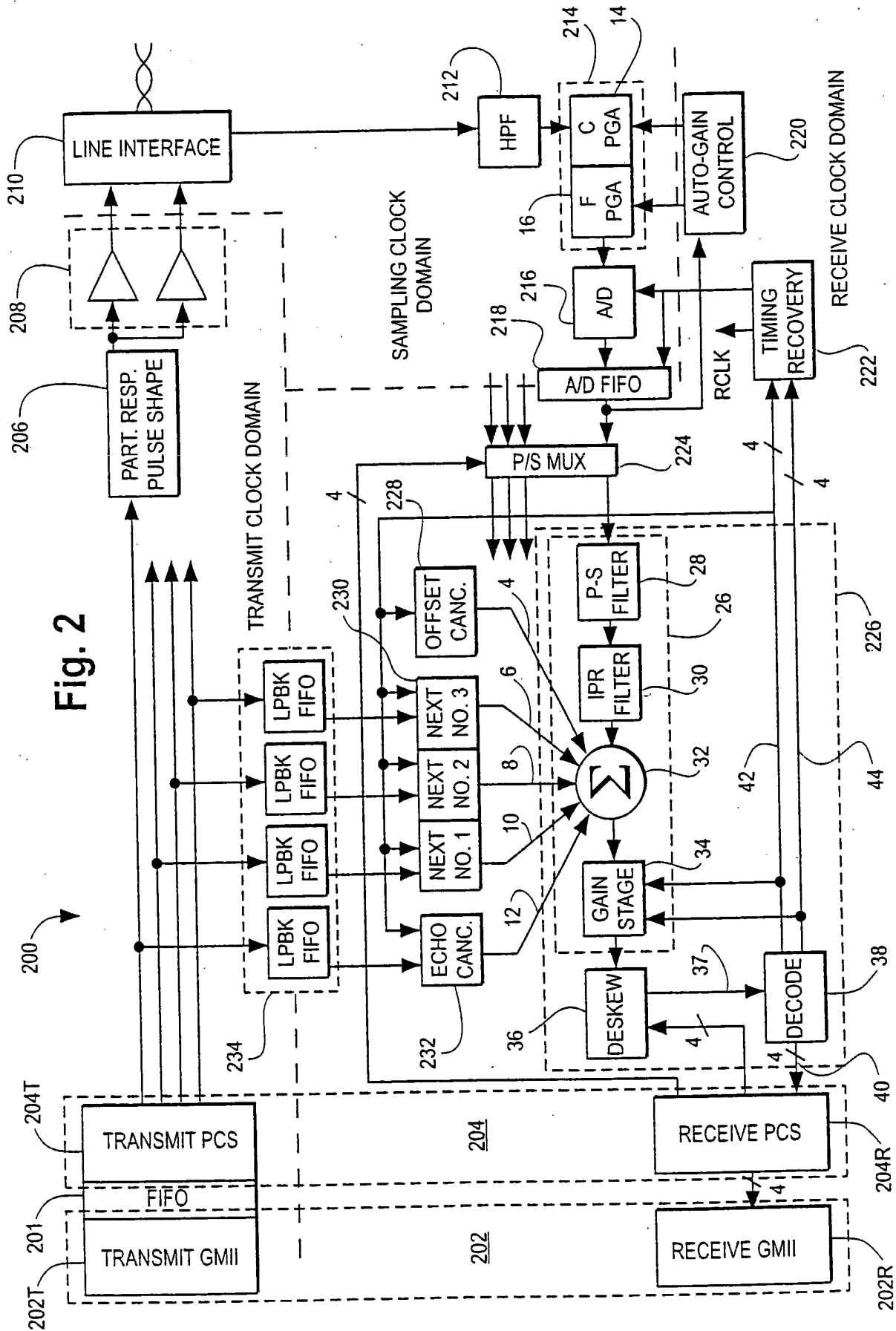


FIG. 3

The diagram illustrates a feedback control system for a line interface. The signal flow is as follows:

- LINE INTERFACE 210**: Receives an external signal (represented by a sine wave) and outputs to the High Pass Filter.
- HIGH PASS FILTER 212**: Filters the signal and outputs to the Course PGA.
- COURSE PGA 16**: Receives a 4-bit control signal from the Automatic Gain Control and outputs to the Fine PGA.
- FINE PGA 14**: Receives a 5-bit control signal from the Automatic Gain Control and outputs to the A/D converter.
- A/D 216**: Converts the analog signal to digital and outputs to the A/D FIFO.
- A/D FIFO 218**: Buffers the digital signal before it is fed back to the Automatic Gain Control.
- AUTOMATIC GAIN CONTROL 220**: Receives a **SET POINT** input and the feedback signal from the A/D FIFO. It generates the 4-bit and 5-bit control signals for the Course and Fine PGAs, respectively.

A dashed box labeled **214** encloses the **COURSE PGA 16** and **FINE PGA 14** blocks.

[illegible]

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FIG. 5

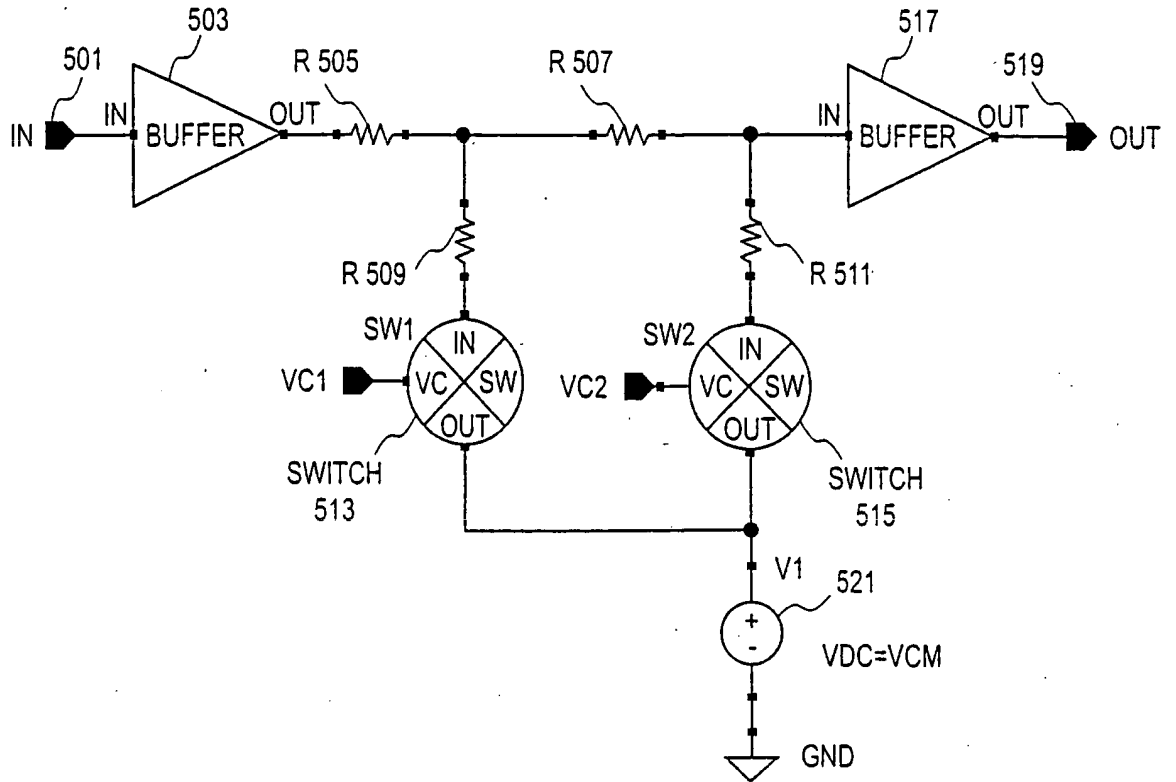


FIG. 6

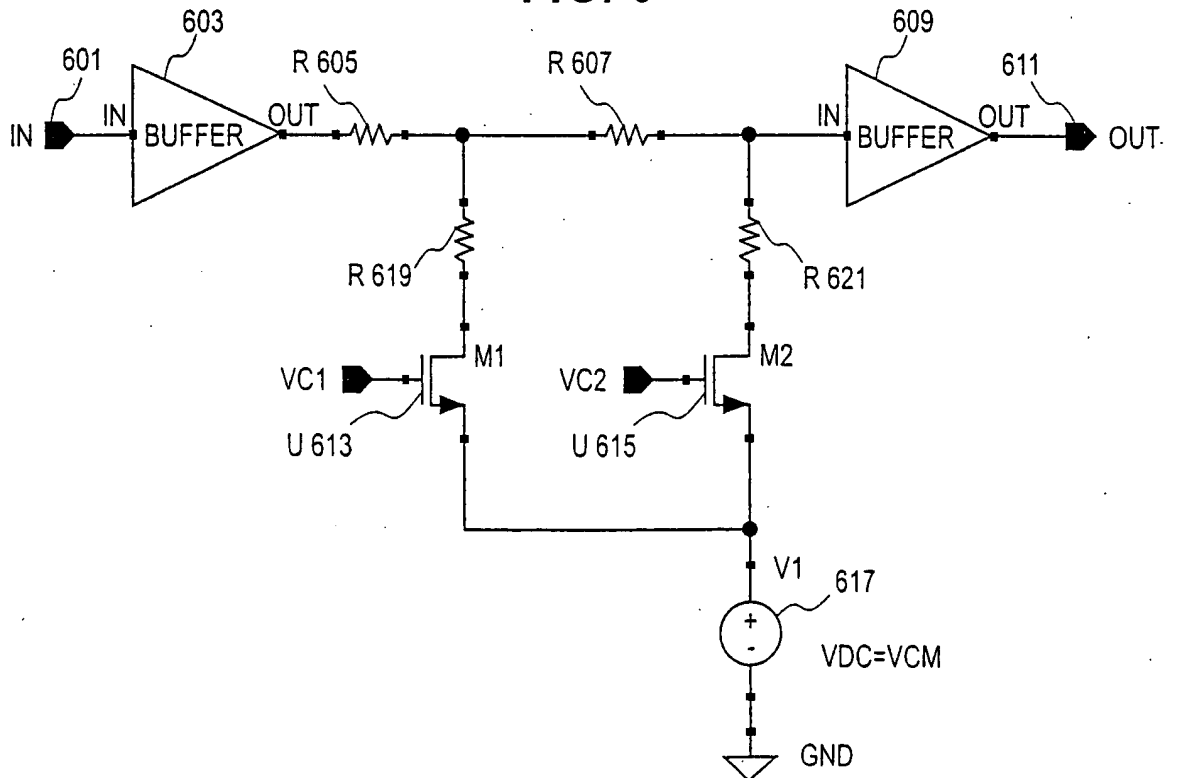


FIG. 7

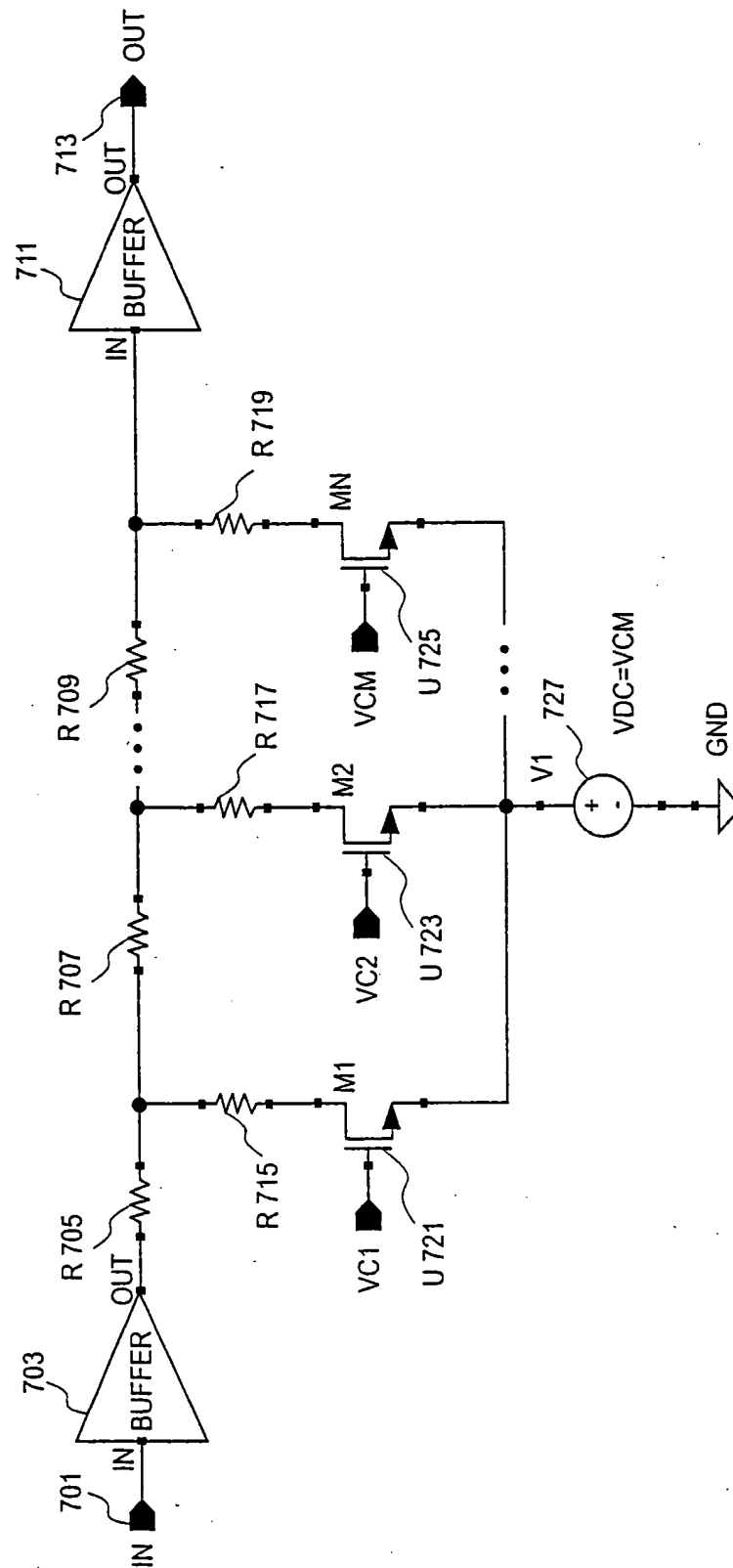
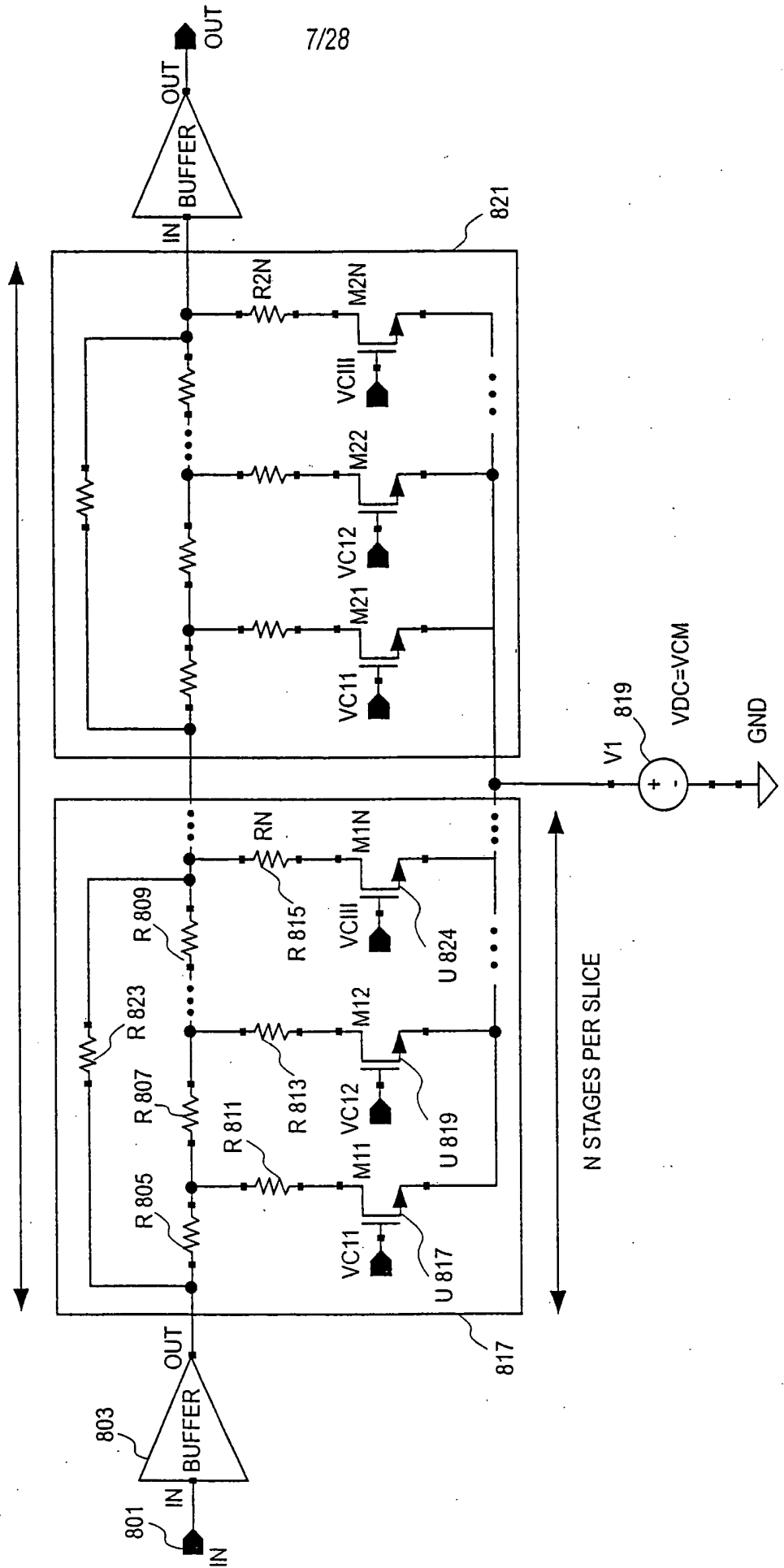


FIG. 8

J SLICES



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FIG. 9

PRIOR ART

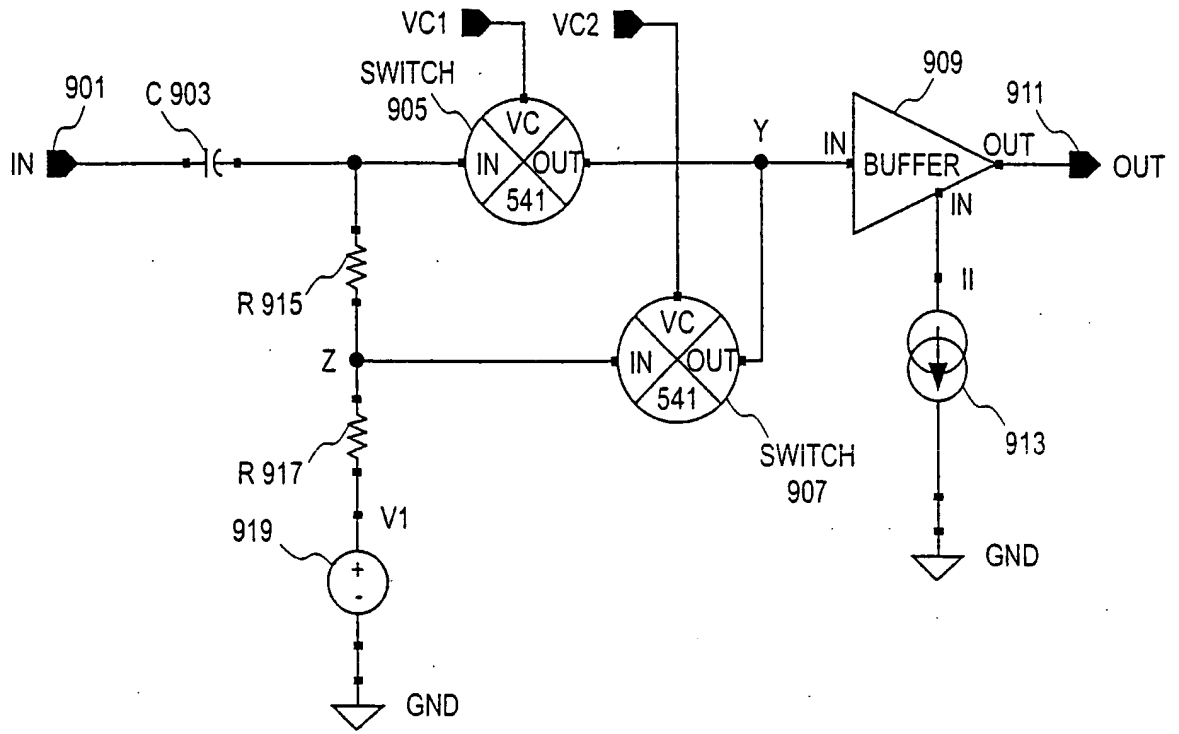
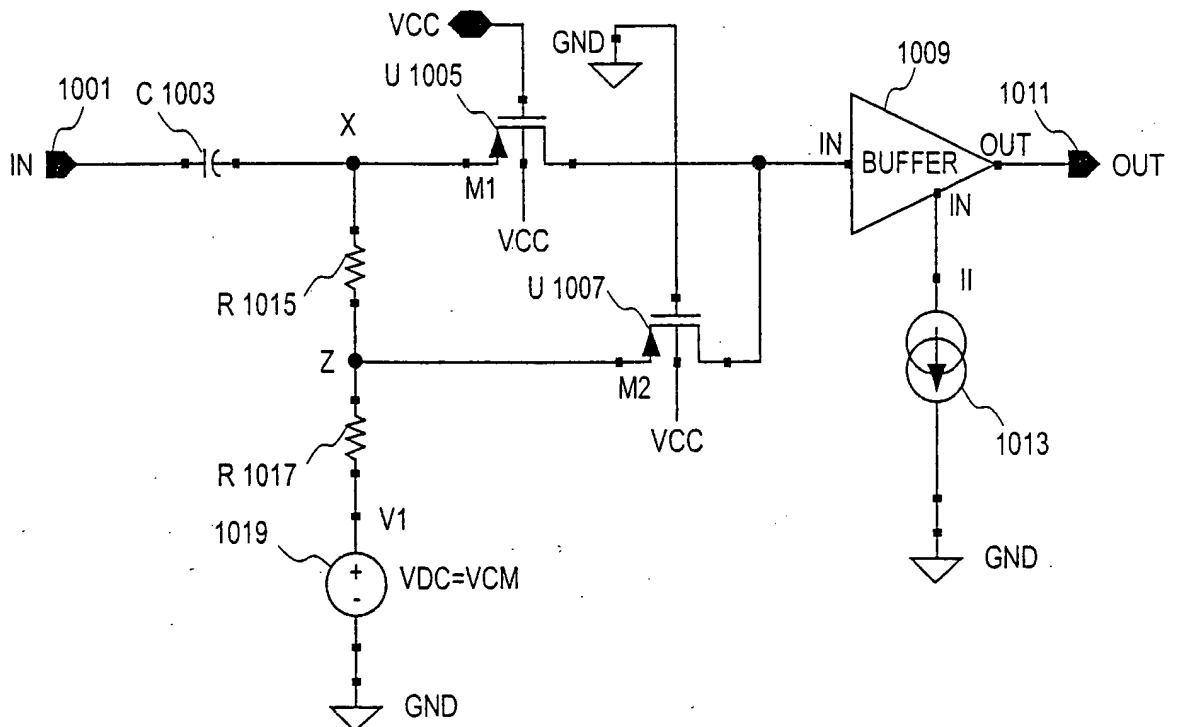


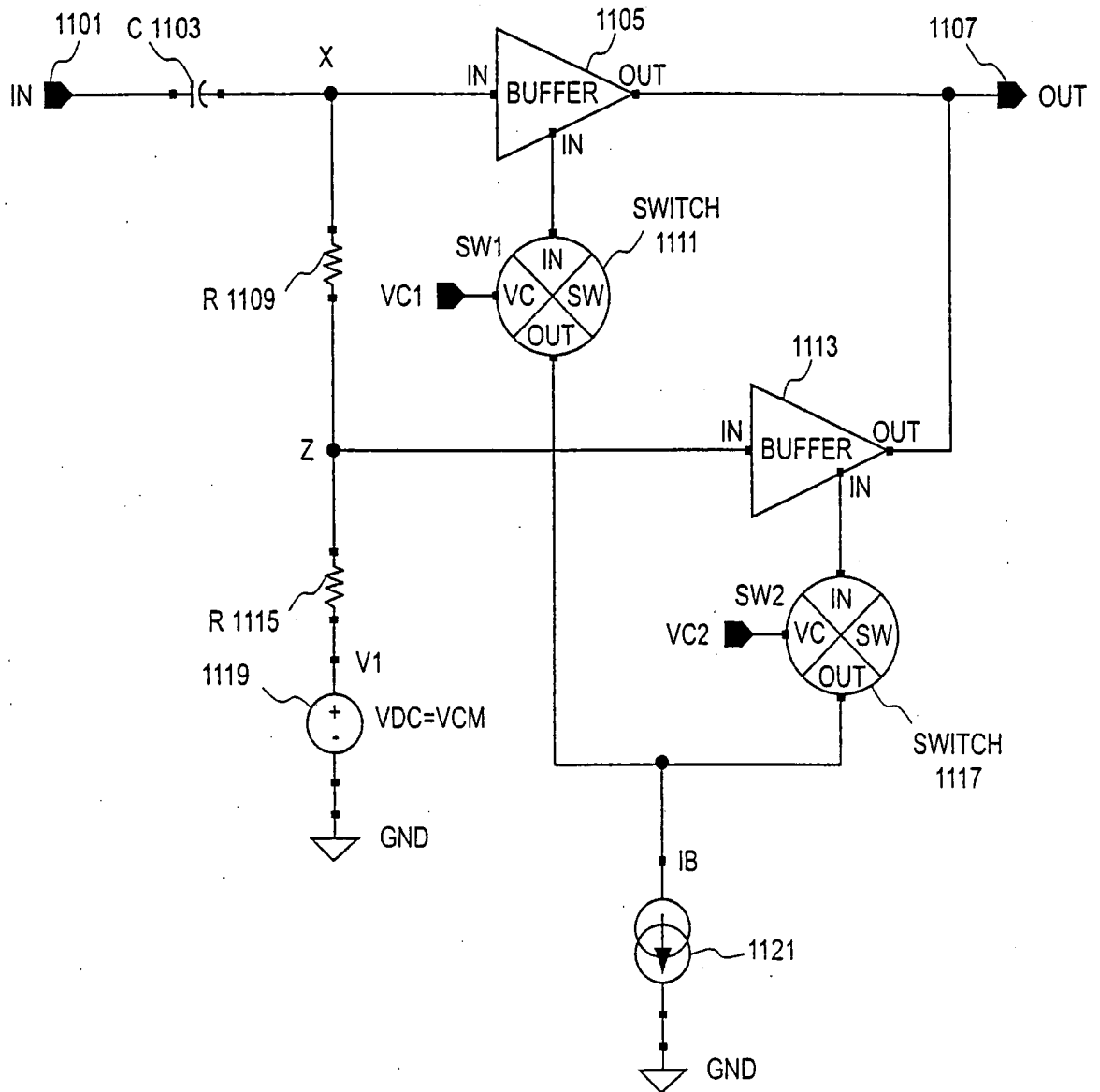
FIG.10

PRIOR ART



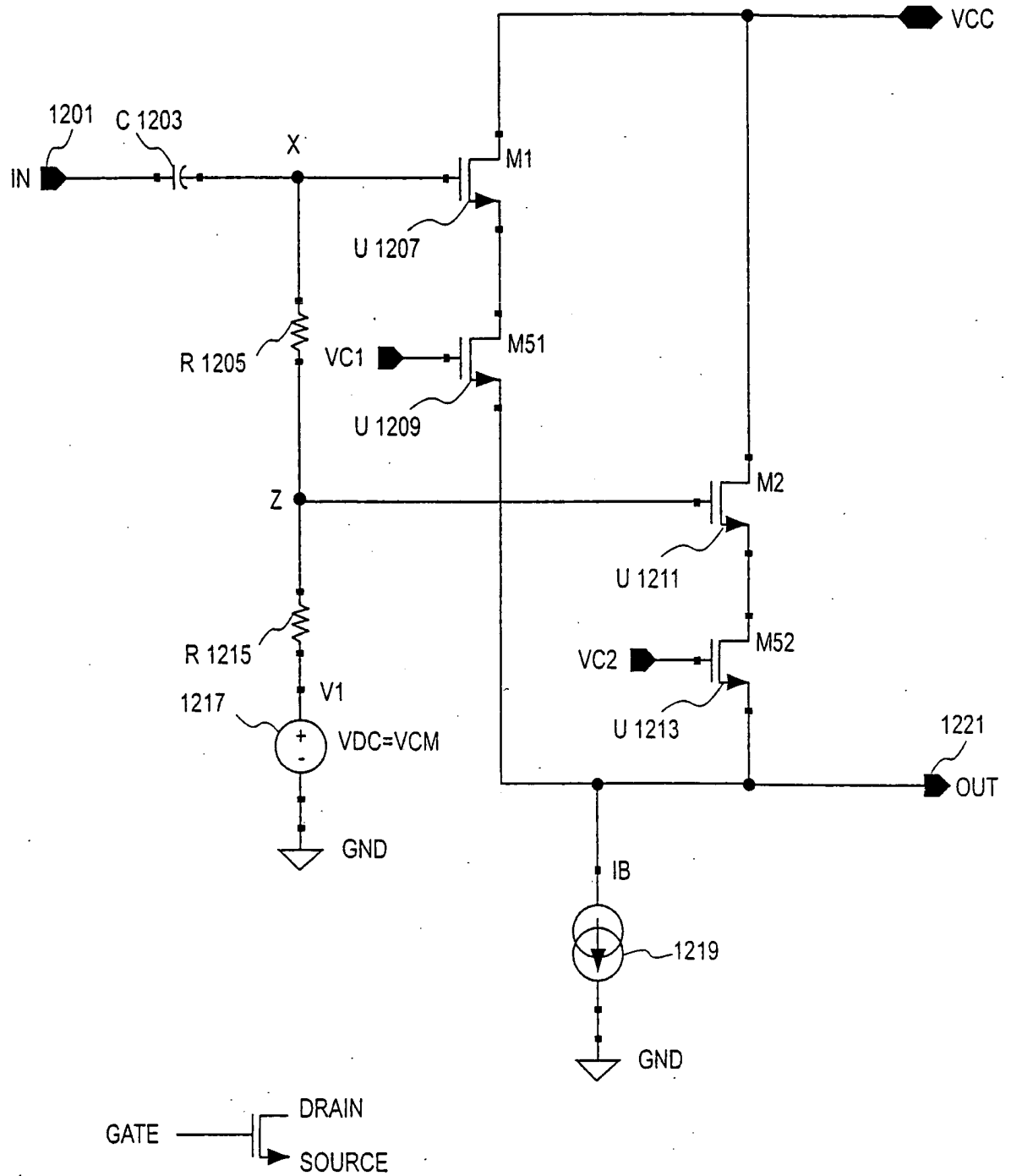
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FIG. 11



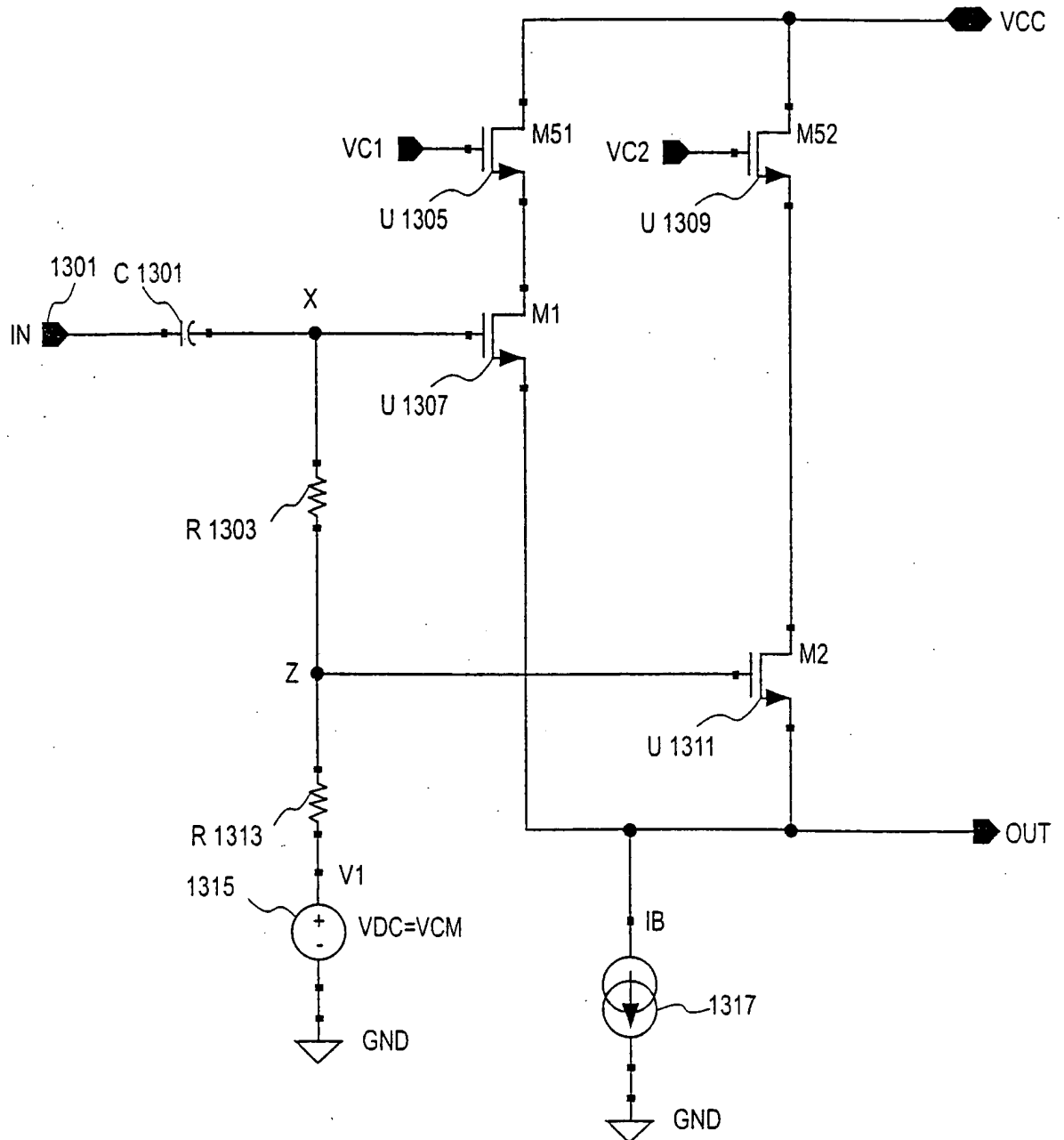
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FIG. 12



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FIG. 13



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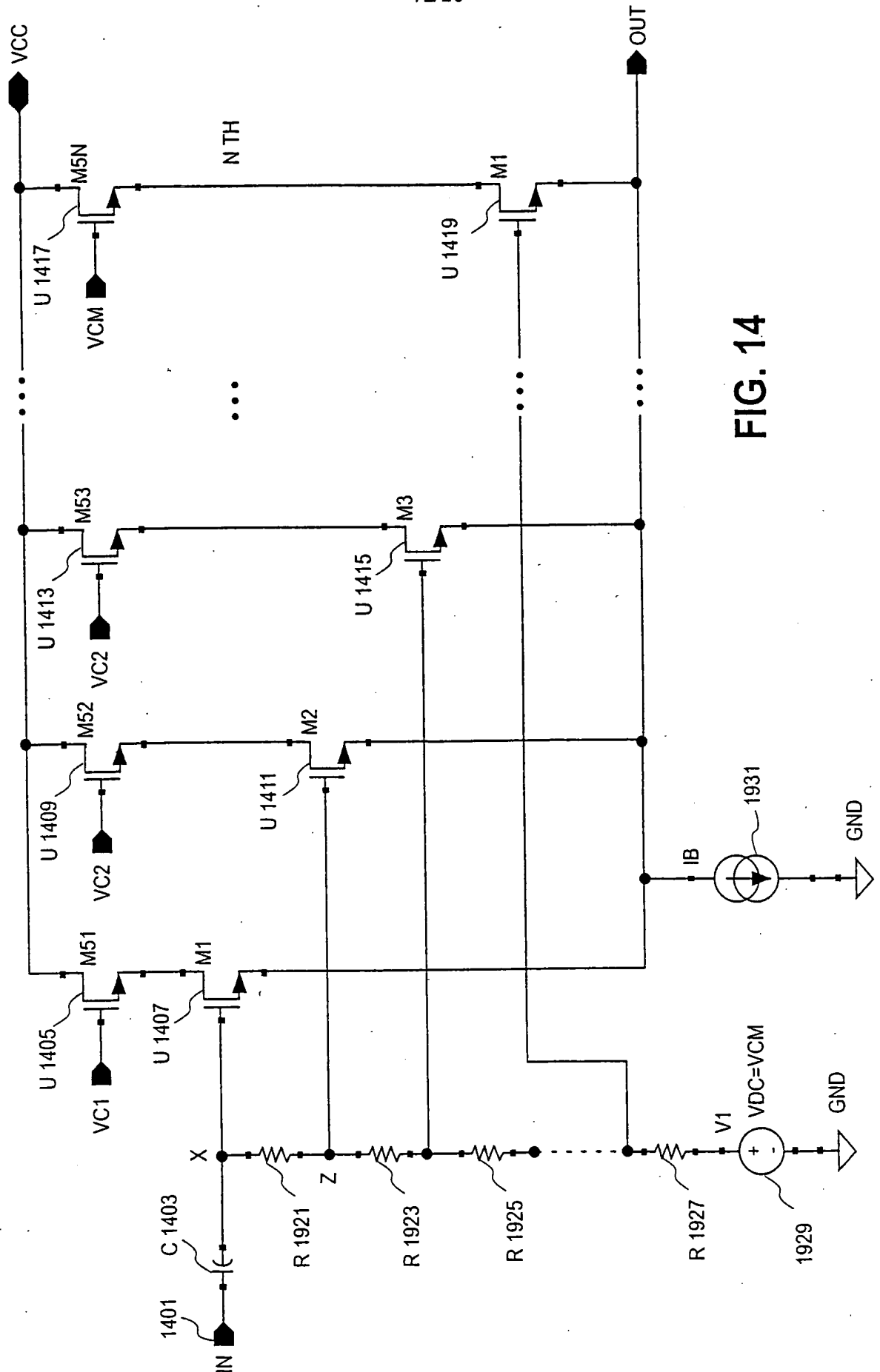


FIG. 14

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FIG. 15

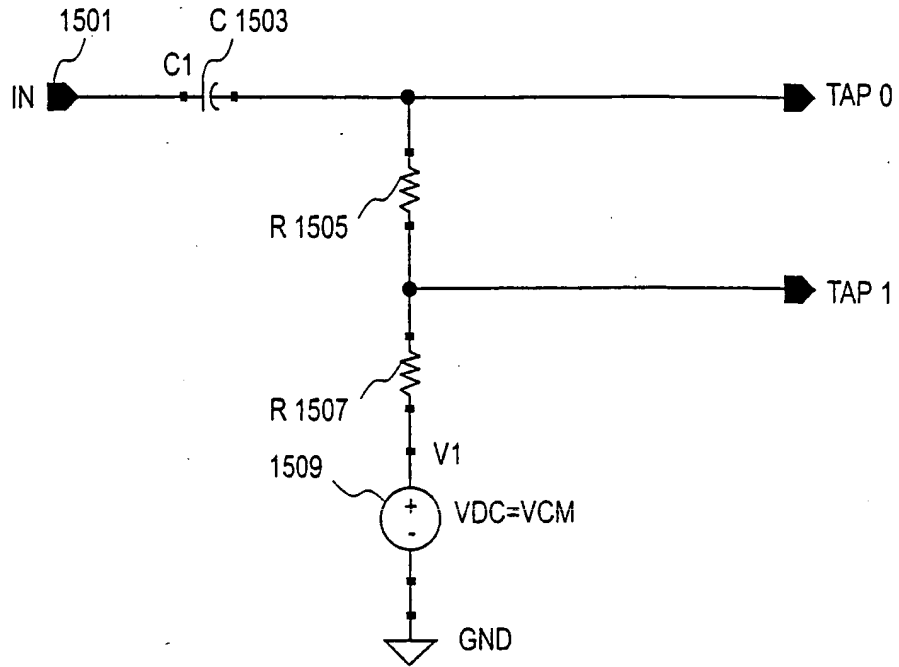
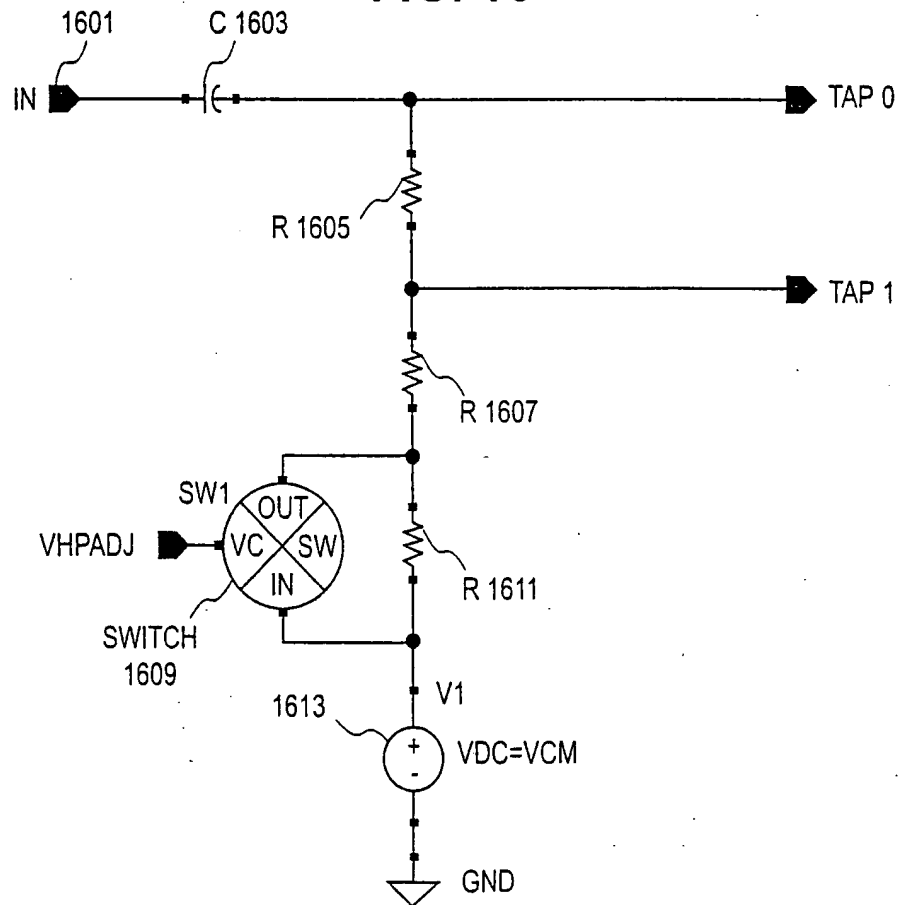


FIG. 16



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FIG. 17

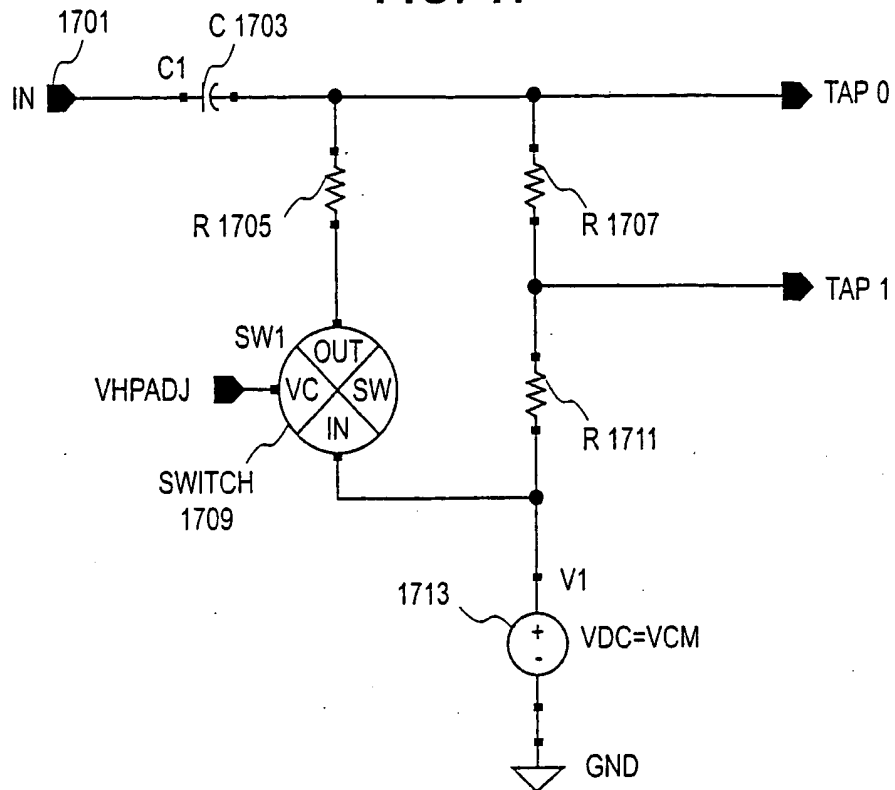
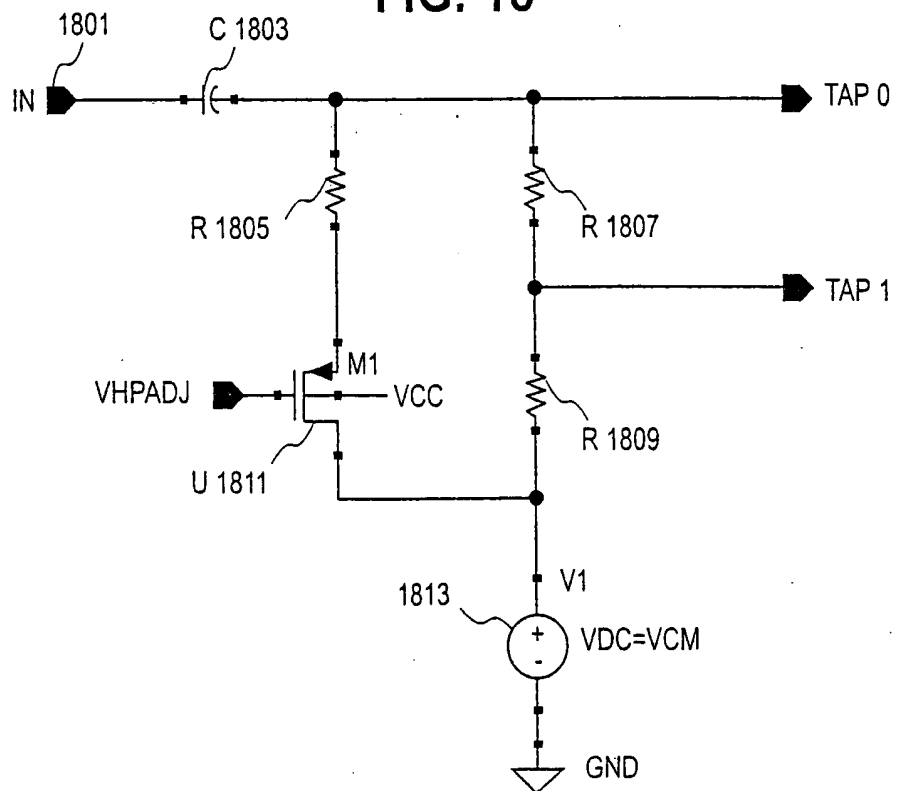
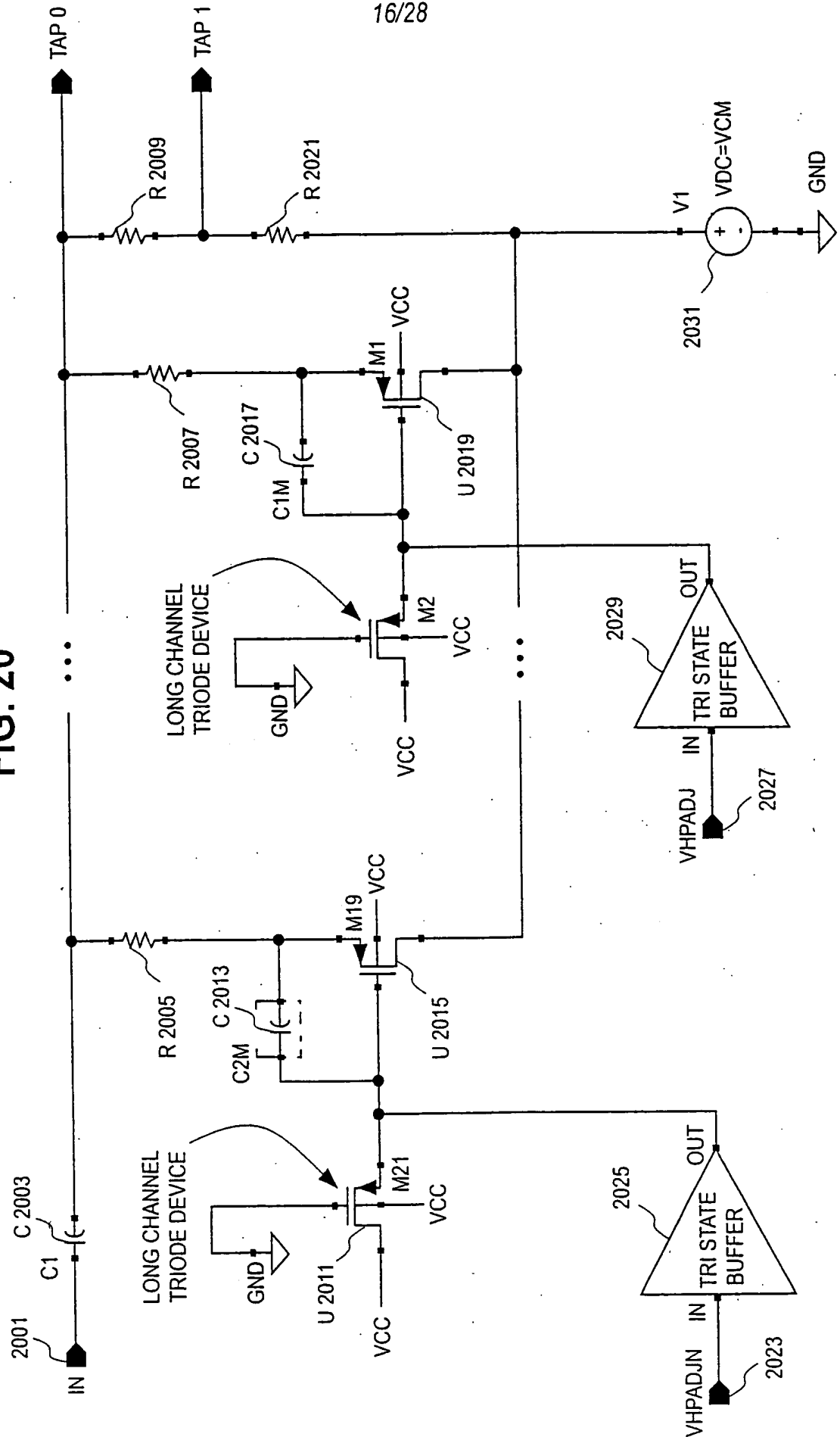


FIG. 18



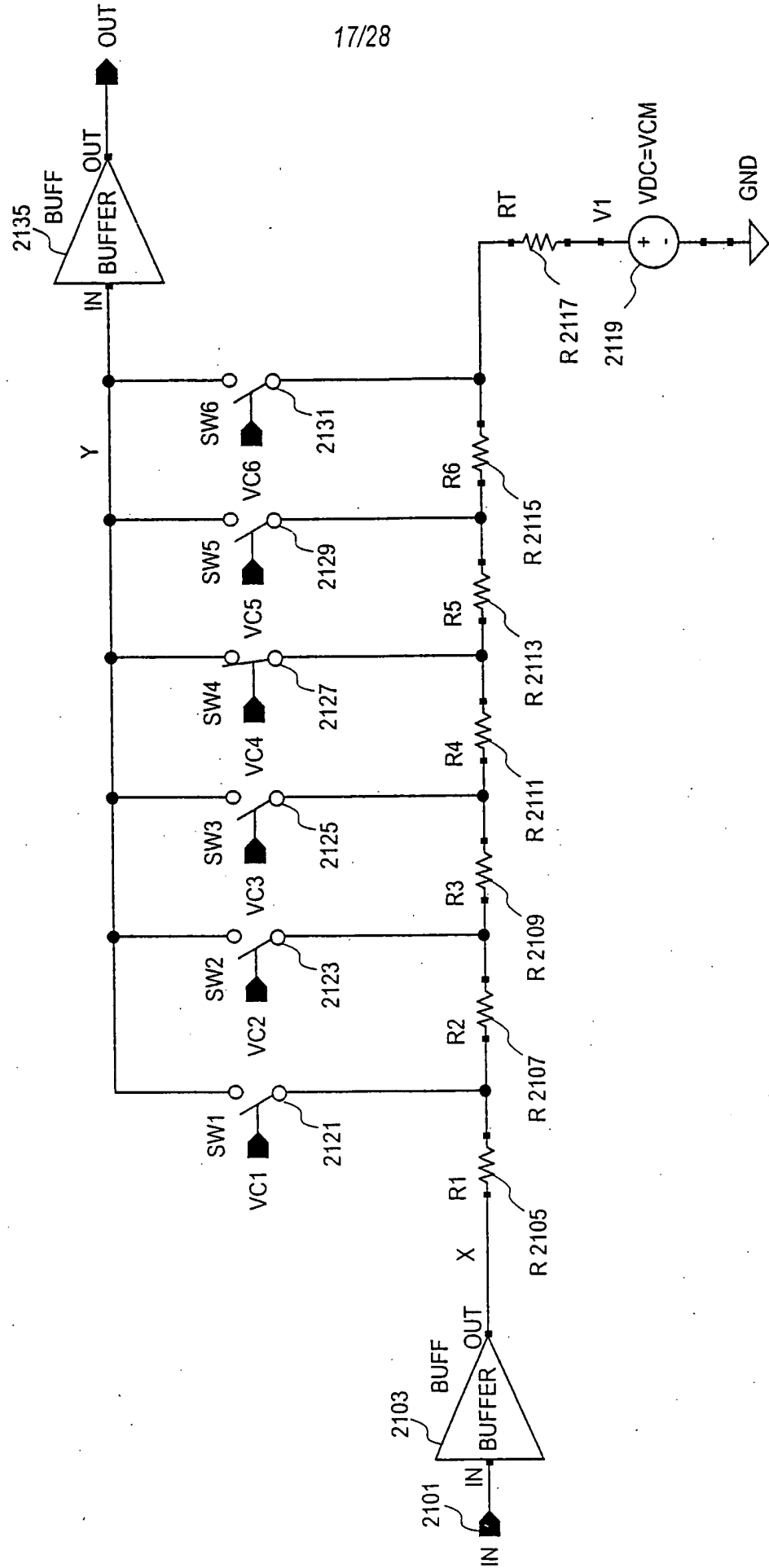
[illegible]

FIG. 20



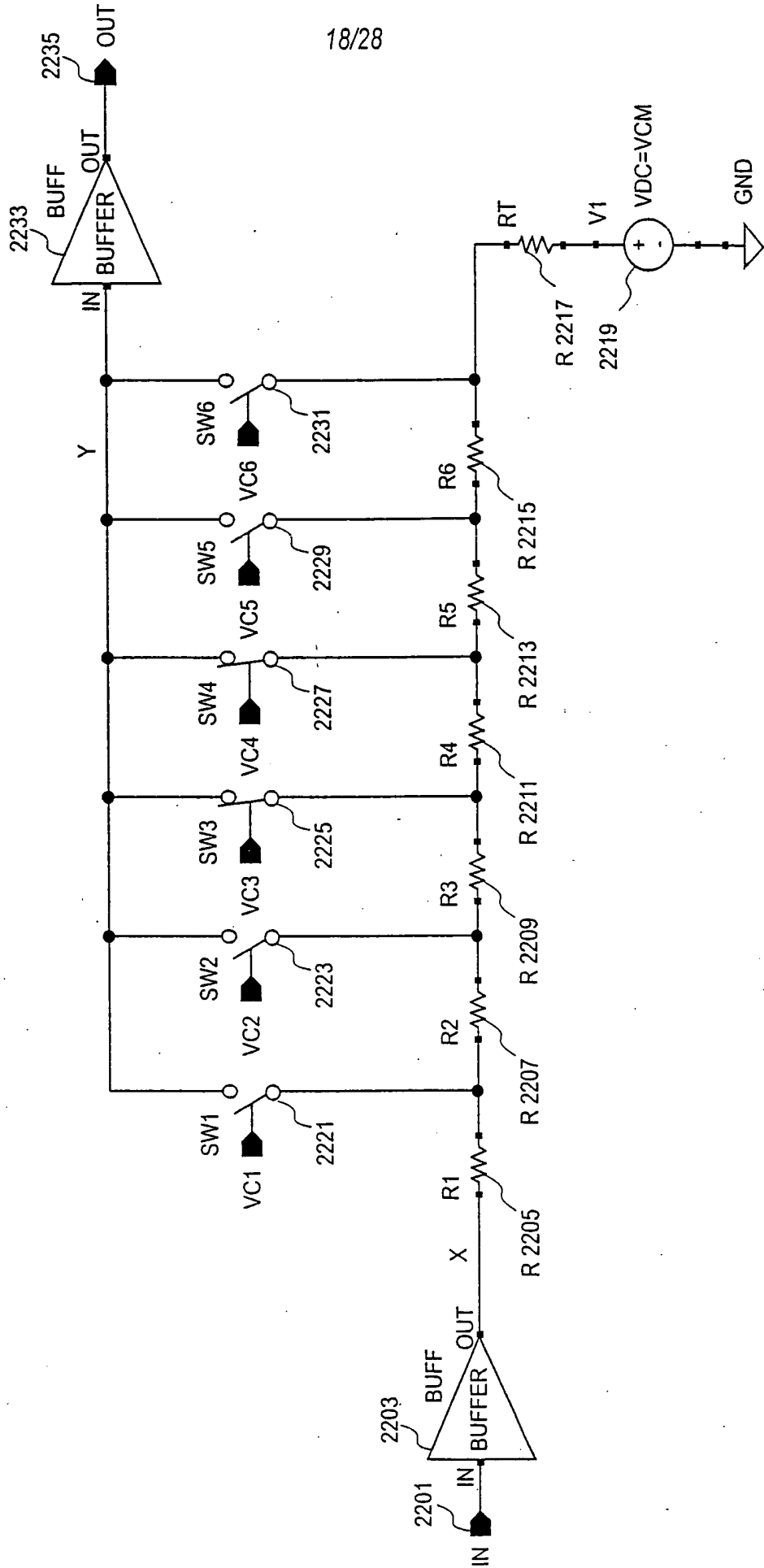
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FIG. 21
 PRIOR ART



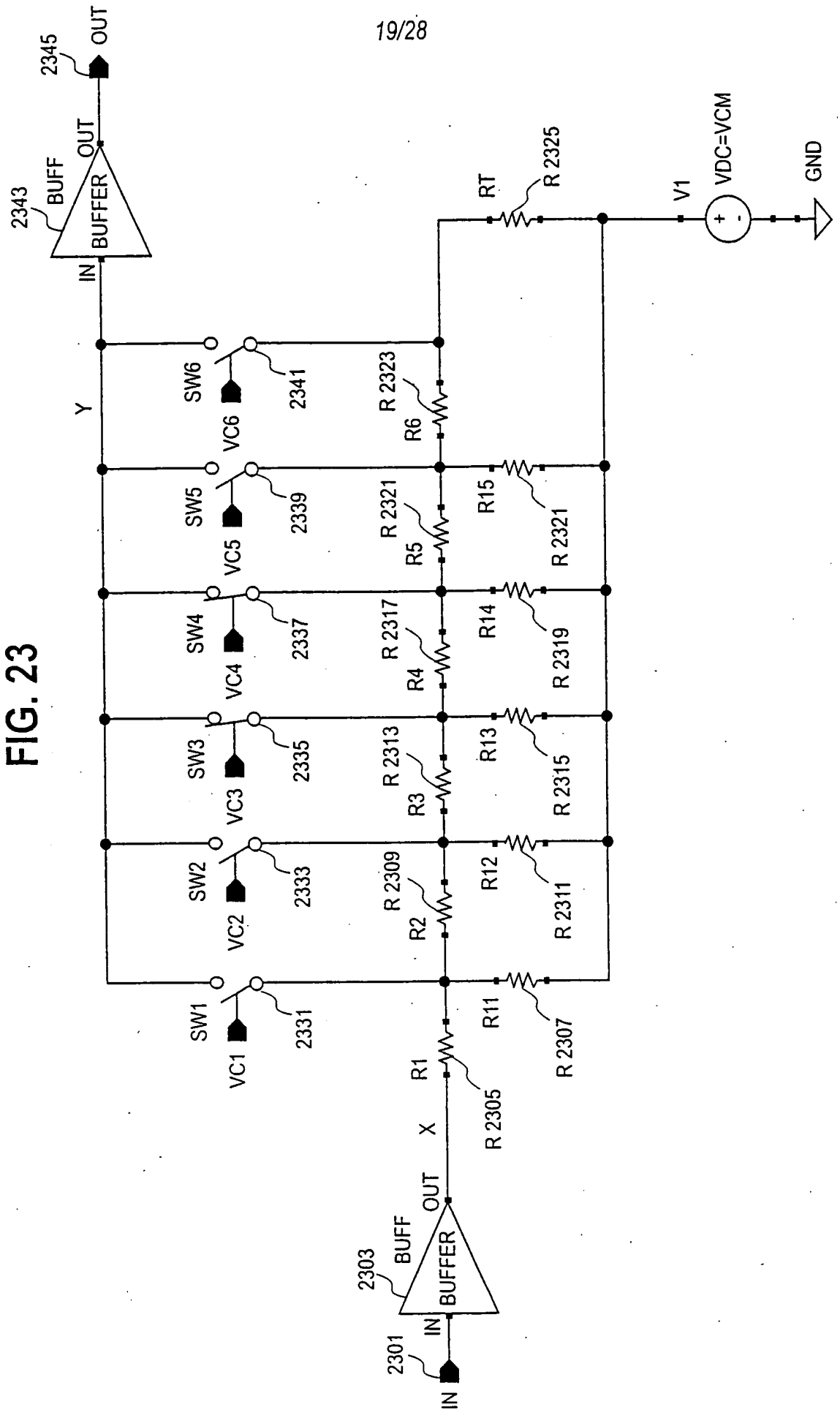
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FIG. 22



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FIG. 23



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FIG. 24

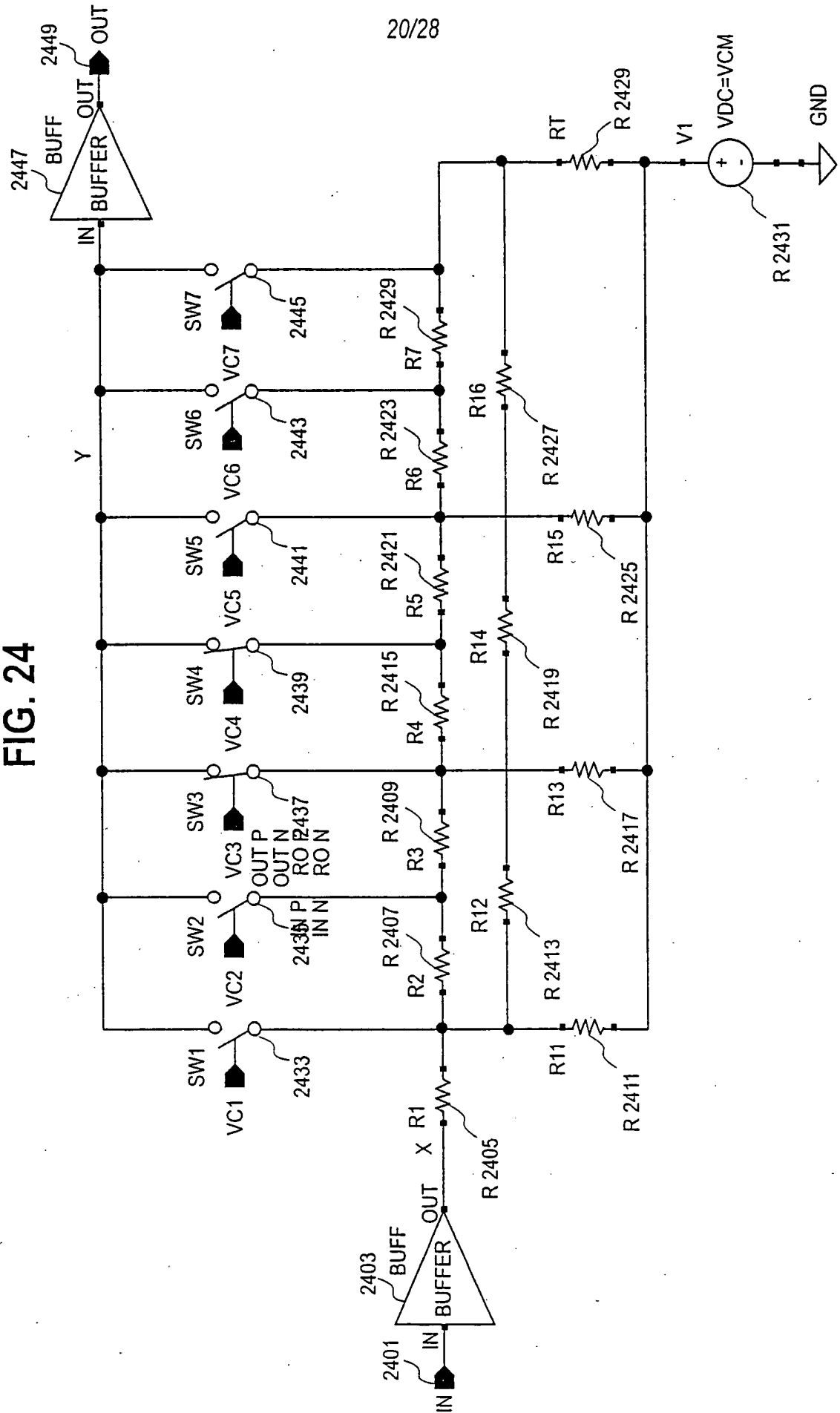
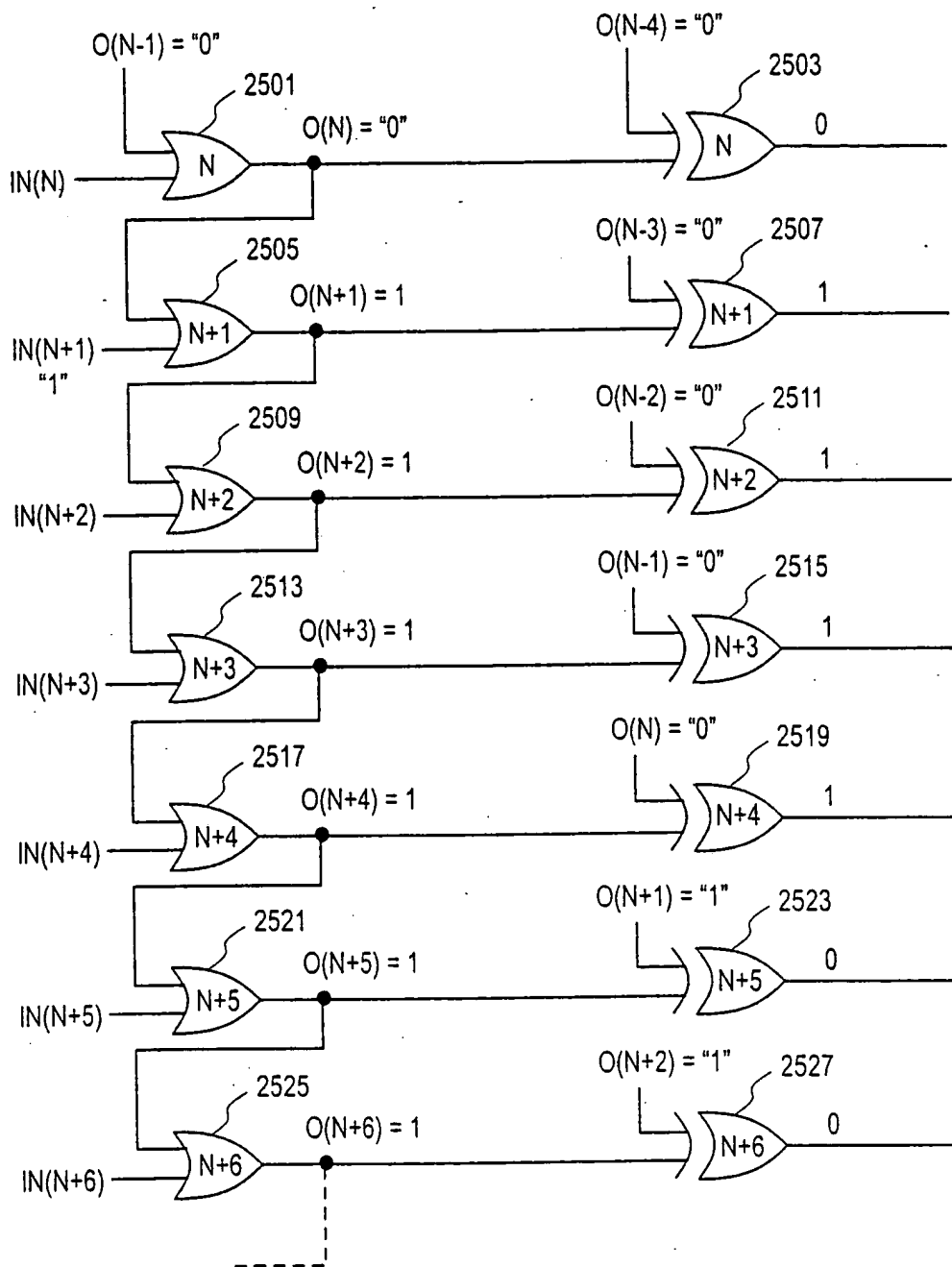
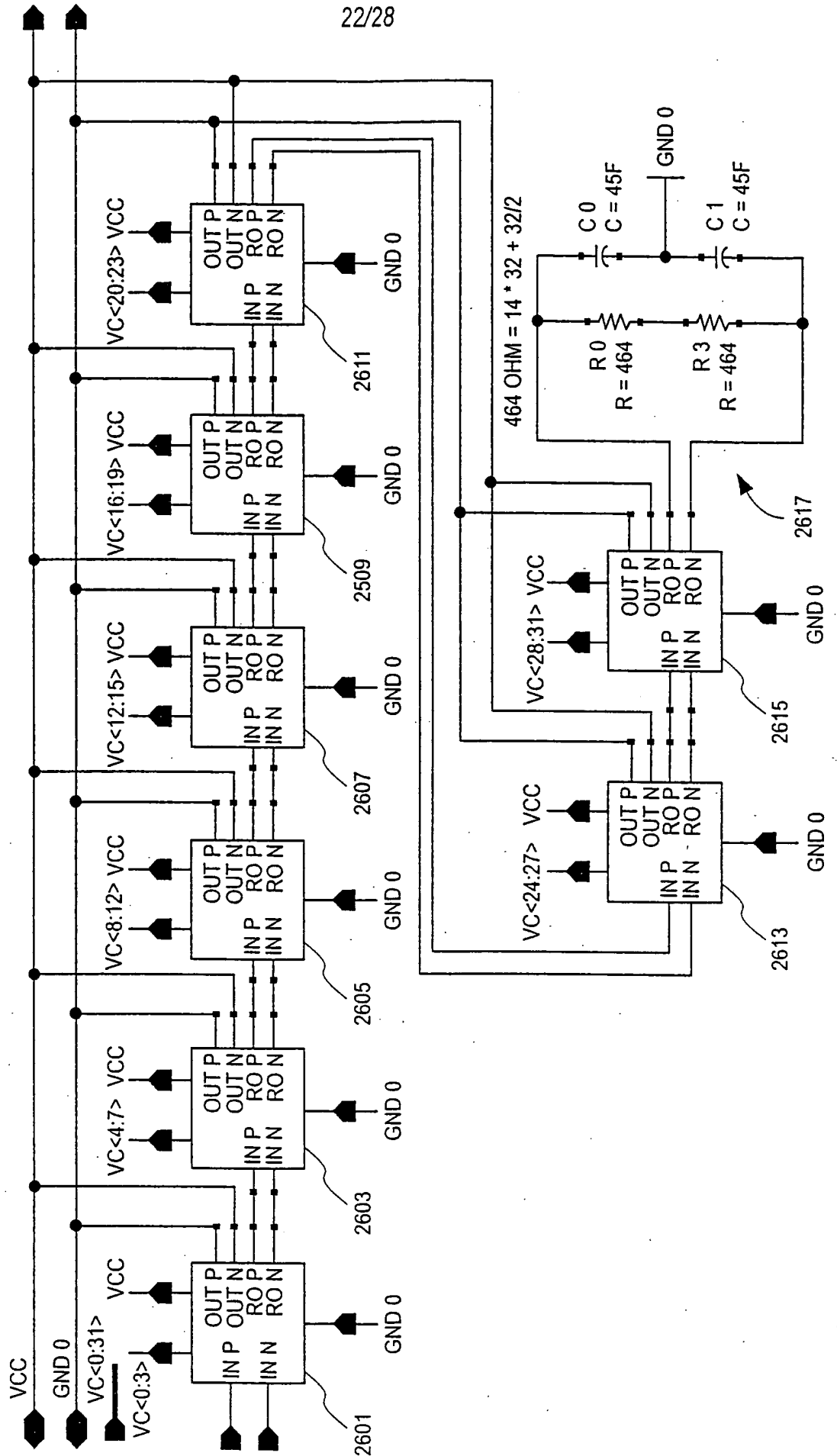


FIG. 25



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FIG. 26



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FIG. 27

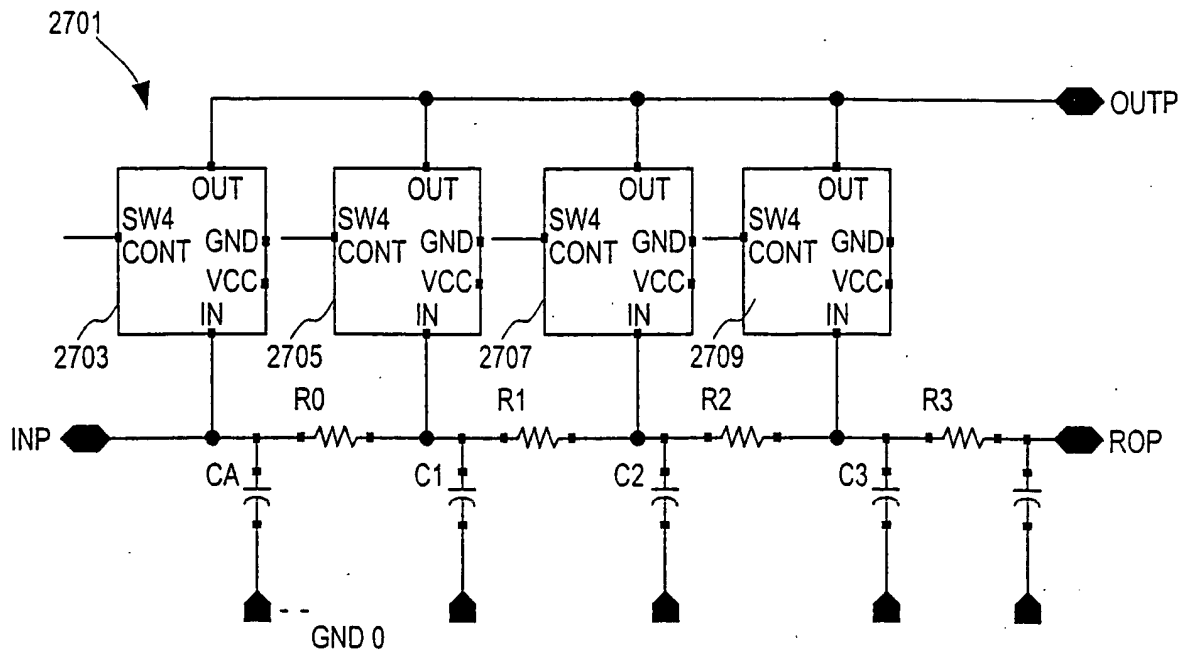
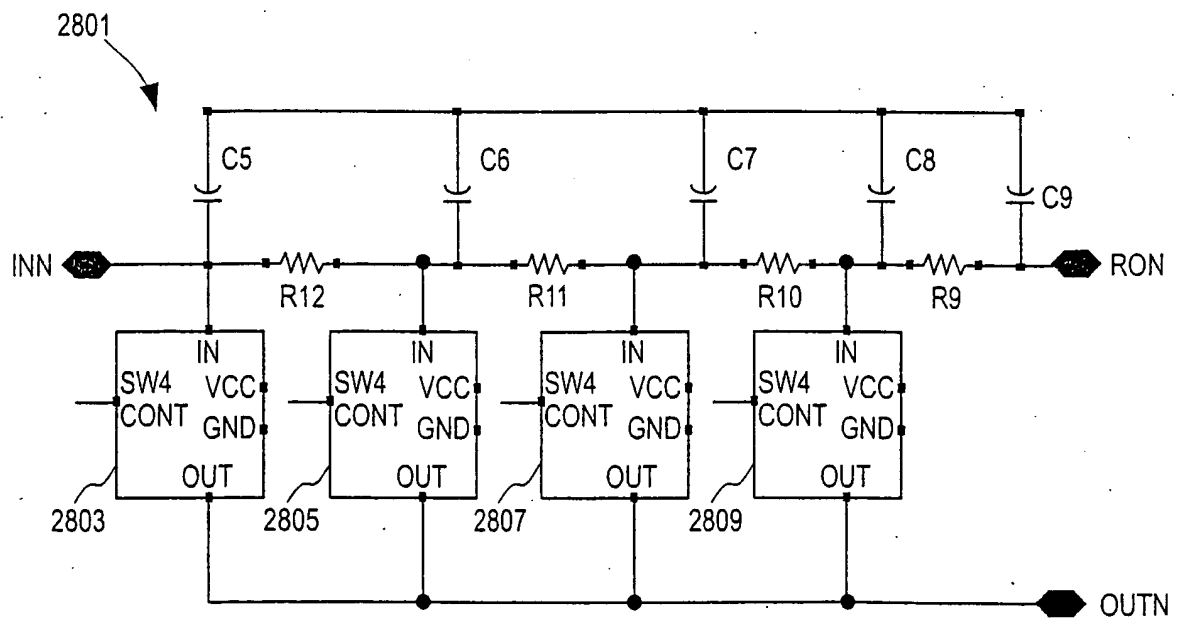
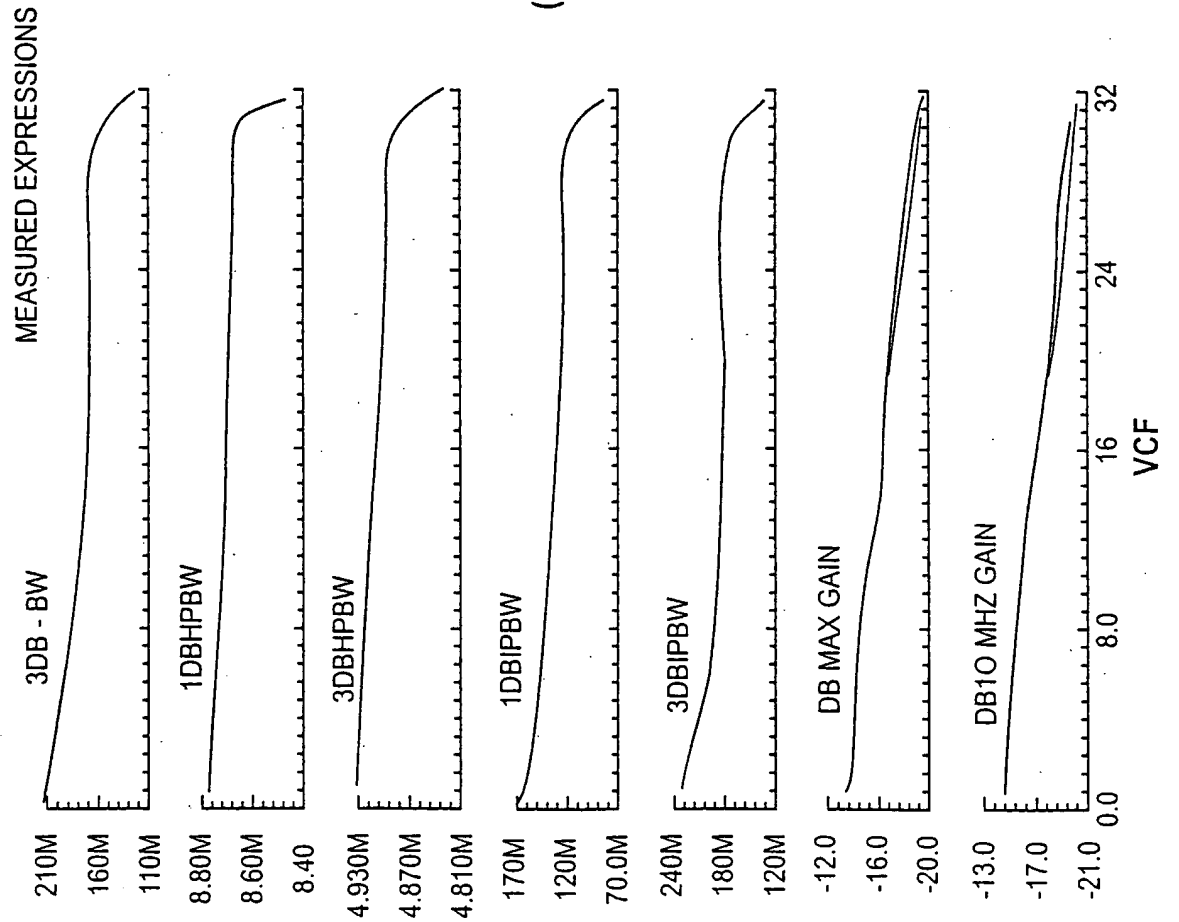
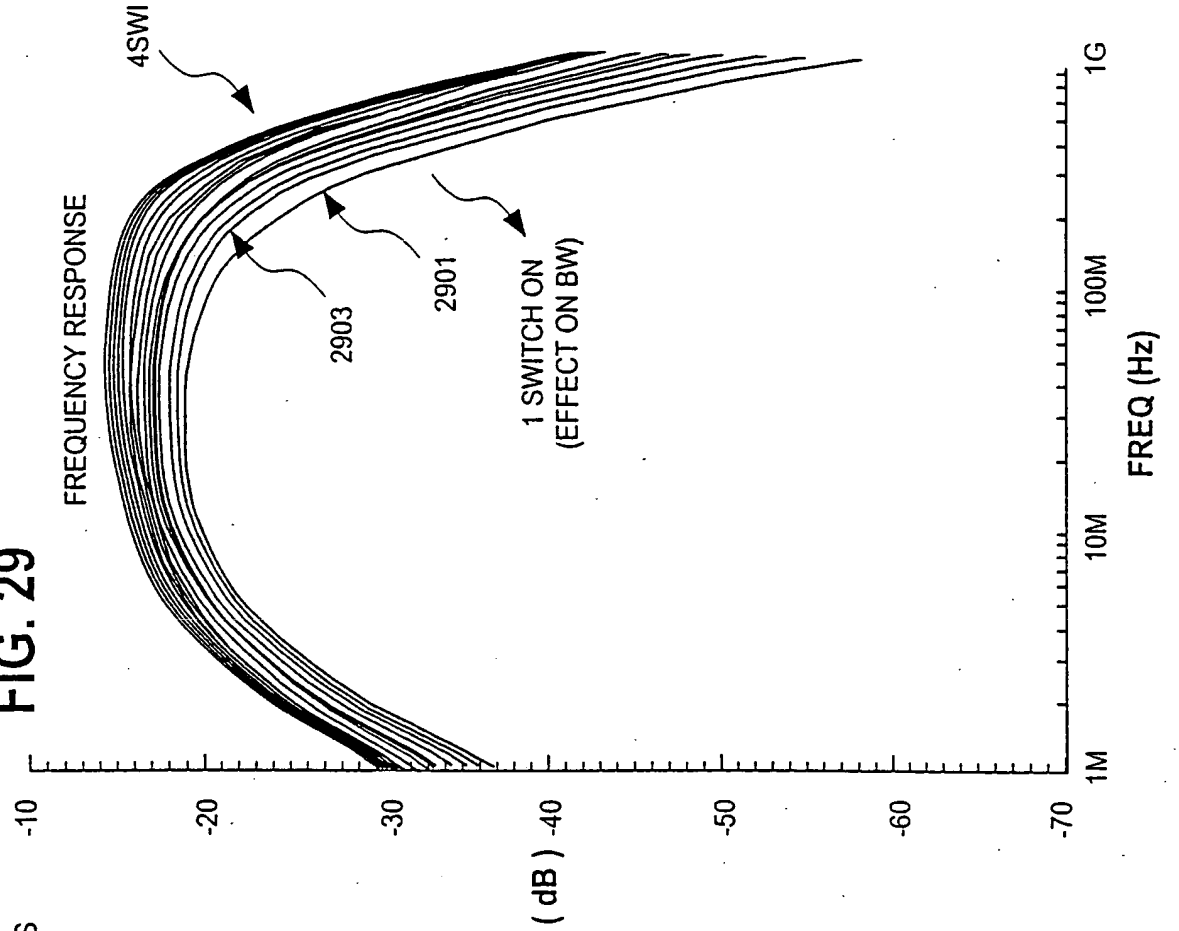


FIG. 28

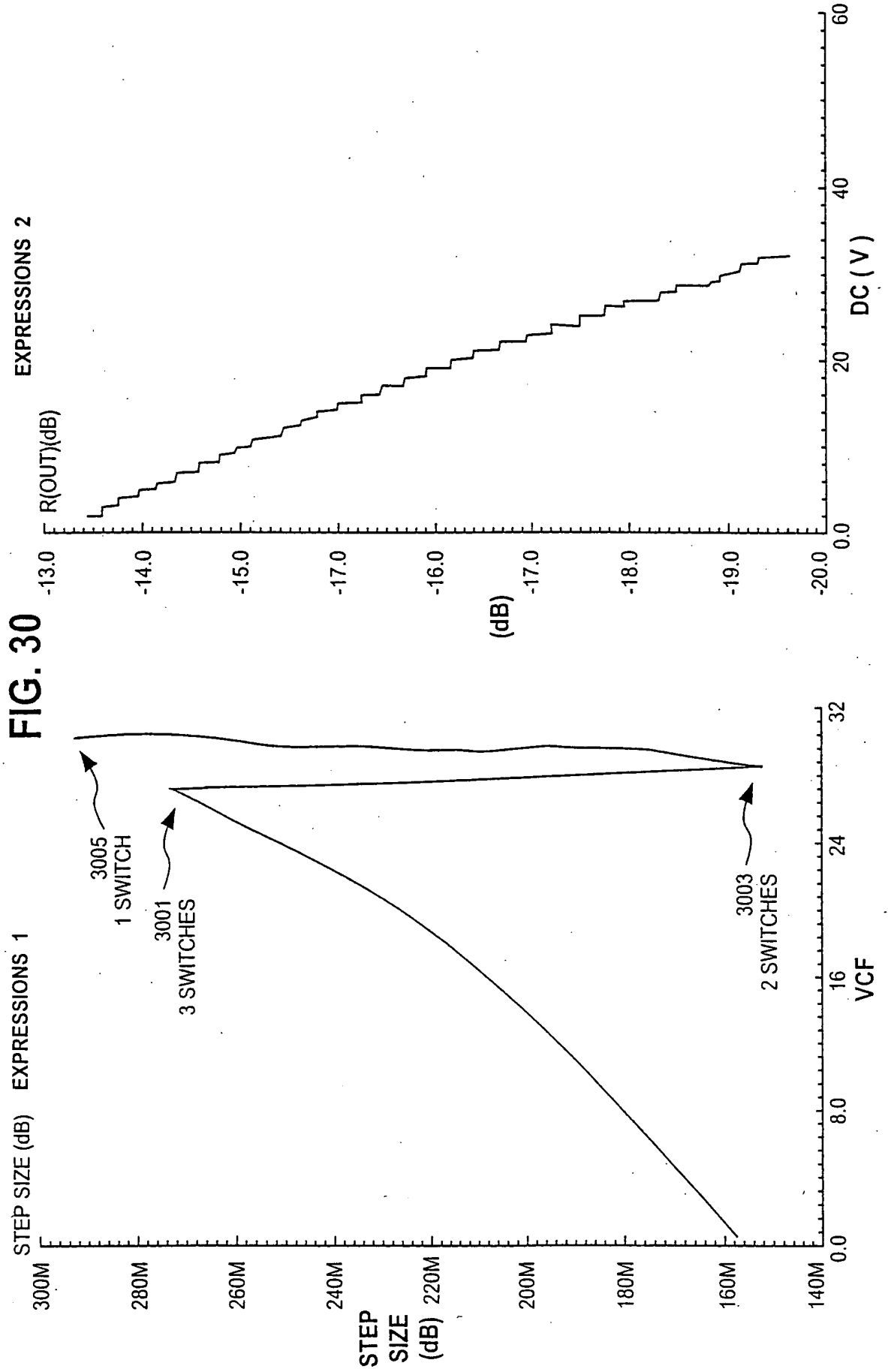


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FIG. 29



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FIG. 31

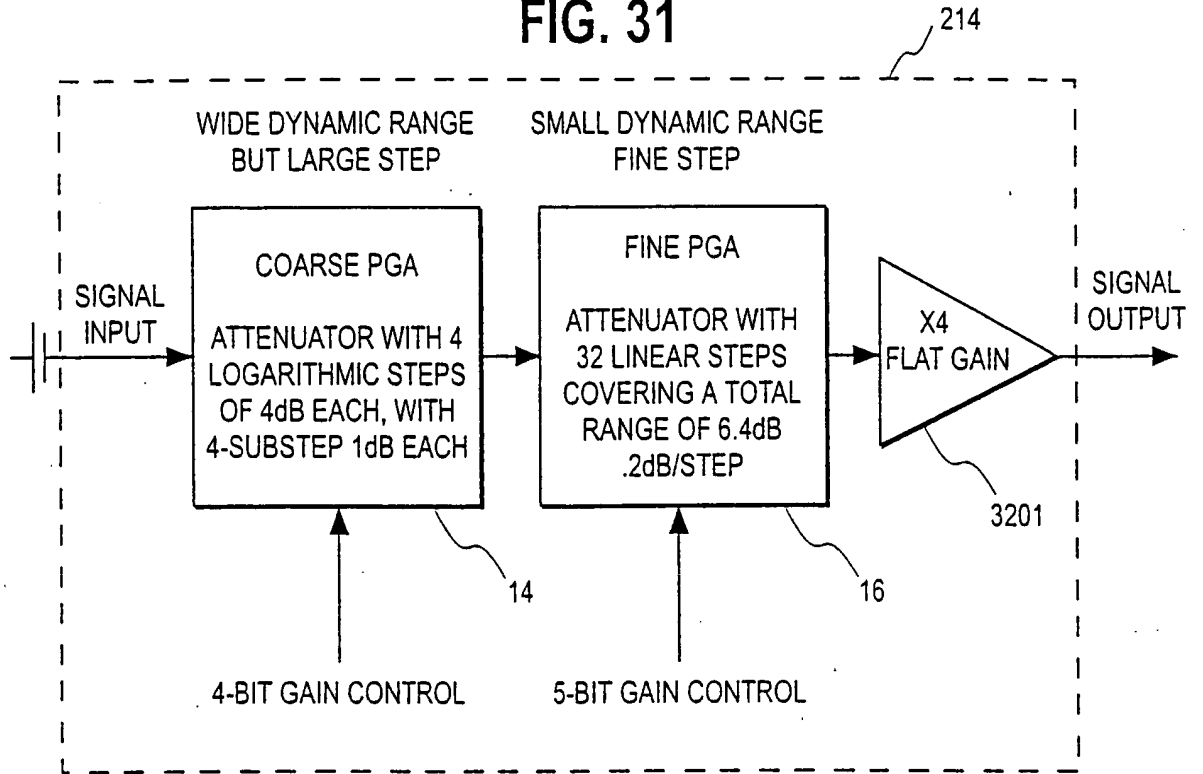


FIG. 32

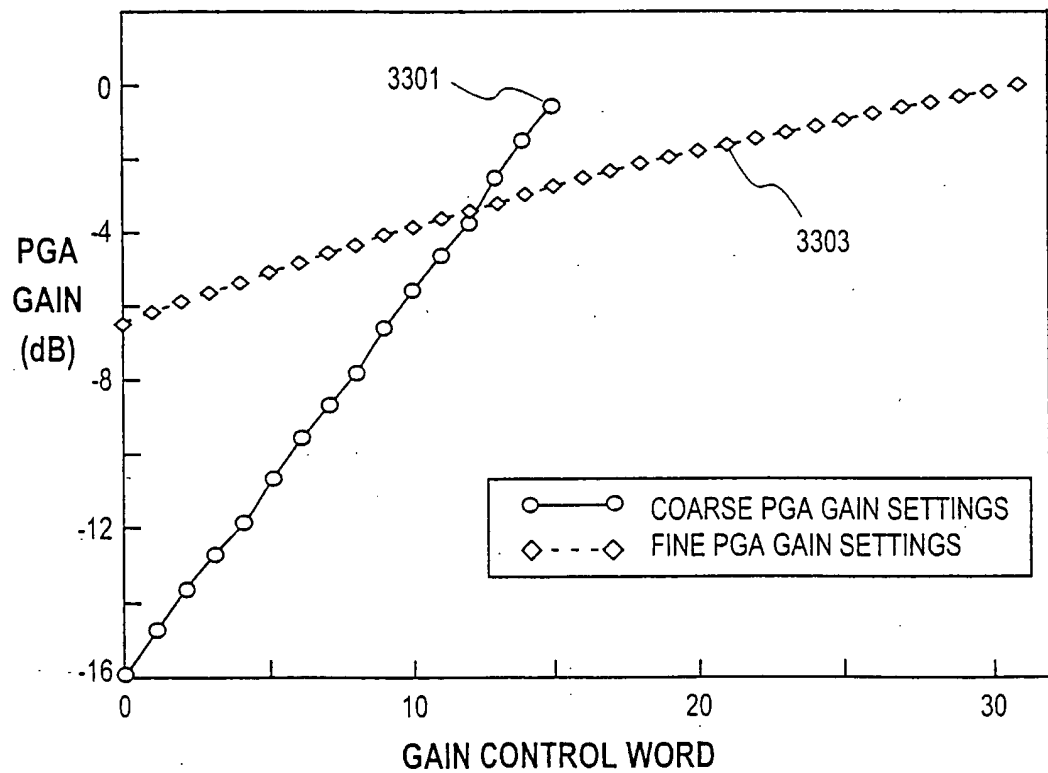


FIG. 33

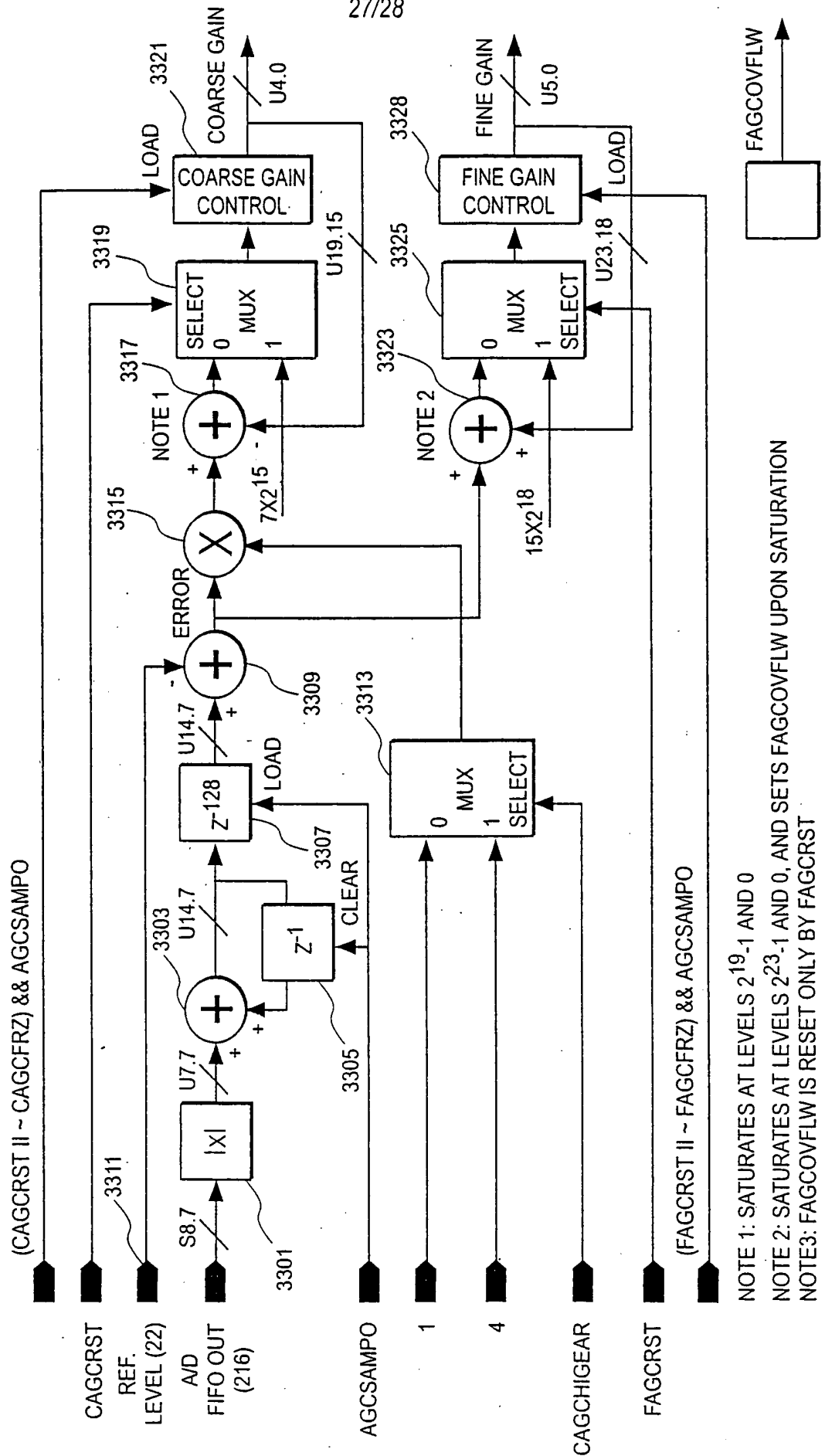


FIG. 34

CABLE LENGTH (m)	100 BASE- TX	GIGABIT, 100 OHM	GIGABIT, 85 OHM	GIGABIT, 115 OHM
0	3.691281	4.193192	4.193192	4.193192
20	3.806628	4.501316	4.362110	4.291369
40	3.877284	4.528136	4.457336	4.429949
60	3.894216	4.733644	4.695307	4.646305
80	4.055372	4.878569	4.847844	4.810019
100	4.225522	4.983545	4.991296	4.968900
120	4.357733	5.134131	5.194401	5.154263
140	4.556012	5.266919	5.380943	5.366309
160	4.764462	-	-	-

$$\begin{aligned}\text{TARGET } E\{IXI\} &= A/D \text{ CLIPPING LEVEL} \times (E\{IXI\}/\text{RMS})/(\text{PEAK}/\text{RMS}) \\ &= 127 \times 0.7979/5.2 = 20\end{aligned}$$